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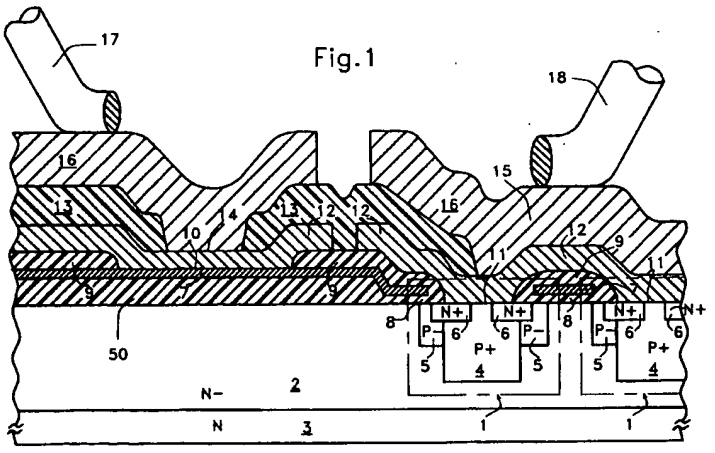
(54) Metallization and bonding process for manufacturing power semiconductor devices.

(57) A metallization and bonding process for manufacturing a power semiconductor device comprises a step of deposition of a first metal layer (12;25) over the entire surface of a chip; a step of selective etching of the first metal layer (12;25) to form desired patterns of metal interconnection lines between components previously defined; a step of deposition of a layer (13) of passivating material over the entire surface of the chip; a step of selective etching of the layer (13) of passivating material down to the first metal layer (12;25) to define bonding areas (14,15;27,28) represented by uncovered portions of the first metal layer (12;25); a step of deposition of a thick second metal layer (16;29) over the entire surface of the chip; a step of selective etching of the second metal layer (16;29) down to the layer (13) of passivating material to remove the second metal layer (16;29) outside said bonding areas (14,15;27,28); and a step of connection of bonding wires (17,18;30,31) to the surface of the second metal layer (16;29) in correspondance of said bonding areas (14,15;27,28).

Fig.1



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The present invention relates to a metallization and bonding process for manufacturing power semiconductor devices.

In the last few years, a fast technological evolution in the field of power semiconductor devices has made available, among the others, power MOSFETs with low values of the "on" resistance ($R_{DS(on)}$), and Power Integrated Circuits (PICs) performing complex functions and capable to switch rather high power values.

PICs are characterized by high levels of components integration density; metal layers should therefore allow a high interconnection density and introduce low series resistances: since these two requirements are in contrast to each other, a trade off value for the thickness of the metal layer must be found. Such thickness values are generally so low that dedicated areas on the die surface, distinct from the active areas wherein the various components are defined, have to be reserved for the attachment (bonding) of leads to the die, as they could perforate the metal layer and damage the underlying integrated circuit. As a result the device area increases, and parasitic resistances due to the necessity of long interconnection lines between the active area and the bonding region are introduced.

Power MOSFETs are less sensitive to integration density problems, but it is extremely important to reduce as far as possible all parasitic resistances so that low values of the $R_{DS(on)}$ can be attained, and thus bond the leads directly on the active area. To prevent the bonding wires from perforating the metallization, this layer should have a rather high thickness, typically greater than 3 µm. Such a thick layer results in problems in both manufacturing and reliability, since the step coverage characteristics of a layer by a superimposed layer get worse as the step height increases.

To prevent damages in the bonding process, the maximum diameter of a bonding wire is generally determined by the metallization layer thickness. To avoid the parasitic resistance of the bonding wire from affecting the MOSFET $R_{DS(on)}$, it is possible to bond in parallel two or more wires of smaller diameter, with an increase in costs.

In view of the state of art just described, the object of the present invention is to accomplish a process for the metallization and bonding of leads to a power semiconductor device, which is not affected by the abovementioned drawbacks.

According to the present invention, such object is attained by means of a metallization and bonding process for manufacturing a power semiconductor device, characterized in that it comprises the following succession of steps:

a) depositing a first metal layer over the entire surface of a chip;

b) selectively etching the first metal layer to form desired patterns of metal interconnection lines between components previously defined;

c) depositing a layer of passivating material over the entire surface of the chip;

d) selectively etching the layer of passivating material down to the first metal layer to define bonding areas represented by uncovered portions of the first metal layer;

e) depositing a thick second metal layer over the entire surface of the chip;

f) selectively etching the second metal layer down to the layer of passivating material to remove the second metal layer outside said bonding areas;

g) connecting bonding wires to the surface of the second metal layer in correspondance of said bonding areas.

The thickness of the first metal layer can be chosen according to the required degree of integration, and is not imposed by bonding requirements. The second metal layer is generally thicker than, but can also have the same thickness as the first metal layer; the thickness of the second metal layer shall be sufficient to prevent its perforation by the bonding wires during the bonding step.

Thanks to the present invention, it is possible to perform the bonding to a PIC chip directly over the active area of the semiconductor substrate wherein the integrated components are obtained, since the overall metallization thickness is at least twice the thickness of the metal interconnection lines. This allows a significant reduction in the chip area, since no dedicated space for bonding is required, and eliminates all the parasitic resistances which would otherwise be present if interconnection lines from the active area to a dedicated bonding area were used.

As far as power MOSFETs are concerned, since the total metallization thickness in the bonding regions is the sum of the thickness of the first and the second metal layers, bonding wires of greater diameter can be used, their low parasitic resistance does not increase significantly the $R_{DS(on)}$ of the device.

With respect to a conventional single metal layer metallization process, the only additional cost is represented by the deposition and definition steps of the second metal layer (i.e. steps e) and f)).

The features of the present invention shall be made more evident by the following detailed description of three particular embodiments, illustrated as non-limiting examples in the annexed drawings, wherein:

Figure 1 is a cross-sectional view of a power MOSFET in which metallization and bonding have been carried out with a process according

to the invention;

Figure 2 is a cross-sectional view of a Power Integrated Circuit wherein metallization and bonding have similarly been carried out accordingly to the invention;

Figure 3 is a cross-sectional view of the power MOSFET of Figure 1, in which metallization and bonding have been carried out with a process according to another embodiment of the invention;

Figures 4-7 are cross-sectional views showing some of the steps of the process according to the invention, applied to the fabrication of the power MOSFET of Figure 1.

With reference to Figure 1, an N-channel power MOSFET is commonly made up of a plurality of elementary cells 1, obtained in an active area region represented by a lightly doped N type epitaxial layer 2, grown over an N type semiconductor substrate 3. Each cell 1 comprises a heavily doped P type body region 4, around which a lightly doped P type annular region 5 is provided, and a heavily doped N type annular region 6 which extends laterally from inside the body region 4 into the P type annular region 5. The N type annular region 6 represents a source region of the elementary cell 1, while the P type annular region 5 is a channel region. A polysilicon layer 7 constitutes the gate electrode of each of the elementary cells 1; said polysilicon layer 7 is isolated from the semiconductor surface by a thin gate oxide layer 8 in the active areas, and by a thicker field oxide 50 elsewhere.

The polysilicon layer 7 is covered by a dielectric layer 9, made for example of silicon dioxide and phosphosilicate glass, in which contact areas 10 and 11 are provided to allow a superimposed first metal layer 12 to contact respectively the polysilicon layer 7 and the surface of the semiconductor in correspondance to each elementary cell 1. The first metal layer 12 can be for example an aluminium-silicon alloy, but different alloys, such as Al-Si-Cu or Al-Si-Ti, could be utilized.

The first metal layer 12, once selectively etched, defines a pattern of interconnection lines between the elementary cells 1.

The first metal layer 12 is covered by a layer 13 of passivating material, such as a phosphosilicate glass, which is selectively removed in correspondance of bonding areas 14 and 15 to allow a superimposed second metal layer 16 to contact the first metal layer 12. The second metal layer 16 has the same composition of but is thicker than the first metal layer 12, in order not to damage the elementary cells 1 during the bonding of wires 17 and 18.

The wire 17 has a smaller diameter than the wire 18 since the current flowing through it (the MOSFET gate current) is much lower than the current flowing through the wire 18 (the MOSFET source current).

A sequence of steps for manufacturing the power MOSFET of Figure 1 according to the process of the present invention is depicted in Figures 4 to 7, wherein all the steps up to the deposition and definition of the first metal layer 12 (Fig. 4) have not been shown being totally conventional.

The layer 13 of passivating material is deposited over the entire surface of the chip (Fig. 5), and is then selectively etched to obtain uncovered portions 14 and 15 of the first metal layer 12 (Fig. 6).

The second metal layer 16 is deposited over the entire surface of the chip, and is successively etched (Fig. 7).

The subsequent attachment of the bonding wires 17 and 18 leads to the structure of Figure 1. No additional passivating layers are necessary, since the surface of the semiconductor is already protected by the layer 13.

The process according to the invention, which has just been described with reference to the fabrication of a power MOSFET, can also be used to obtain different power devices, for example Power Integrated Circuits (PICs).

Figure 2 shows the cross-section of a typical PIC. A heavily doped N type buried layer 20 is implanted into a lightly doped P type substrate 19, and a lightly doped N type epitaxial layer 21 is grown over the surface of the substrate 19. The epitaxial layer 21 represents an active area region wherein various integrated components are obtained, such as three elementary cells 22 of a power MOSFET.

Heavily doped P type and N type regions 23 and 24 are obtained by implantation into the epitaxial layer 21 and allow the formation of contacts to the P type substrate 19 and to the buried layer 20, respectively.

The elementary cells 22 are identical to the already described elementary cells 1 of Figure 1.

A first metal layer 25, properly patterned by selective etching, contacts each of the cells 22, their polysilicon gate layer 7, the P type region 23 and the N type region 24. Superimposed over the first metal layer 25, a layer 26 of passivating material, e.g. phosphosilicate glass, is etched to expose portions 27 and 28 of the first metal layer 25, which represent bonding areas for the chip.

A second metal layer 29, deposited over the entire surface of the chip, contacts the underlying first metal layer 25 in correspondance of said uncovered portions 27 and 28. After the selective etching of the second metal layer 29, wires 30 and 31 are bonded to it in correspondance of the bonding areas.

The thickness of the first metal layer 25 is determined by the required components integration density. The second metal layer 29 is thicker than the first metal layer 25, so that during the bonding of wires 30 and 31 it is not perforated, allowing to perform the bonding directly over the active area regions, while not affecting the components integration density.

It is also possible, without changing the process sequence of steps but only the layout of the intermetal dielectric mask, to improve the reliability of the bonding.

Figure 3 shows again the power MOSFET of Figure 1. The only difference with respect to Figure 1 is given by the presence of two islands 32 of passivating material, obtained during the etching of the layer 13 (step d)) by using a mask with a different layout with respect to the one used in the case of Figure 1. Such islands generate a roughening of the surface of the second metal layer 16, thus increasing the friction between the bonding wire 18 and the surface of the second metal layer 16 during the bonding step. This improves the adherence of the bonding wire, and the device is thus made more reliable. In a preferred embodiment the islands 32 can be distributed over the bidimensional array of elementary cells 1 and separated by a distance corresponding to the diameter of the bonding wire 18.

In Figure 3, no islands of passivating material are provided in the bonding region 14 of the bonding wire 17 since this is connected to the gate electrode and must conduct smaller currents with respect to the wire 18 connected to the source of all the elementary cells 1. The wire 17 has therefore a smaller diameter, and its bonding to the surface of the second metal layer 16 is consequently less critical.

It is evident to anyone skilled in the art that the process according to the invention is not limited in its application to power MOSFETs or PICs, but can be employed in the manufacturing of any other power semiconductor device, such as Insulated Gate Bipolar Transistors (IGBTs).

Claims

1. A metallization and bonding process for manufacturing a power semiconductor device, characterized in that it comprises the following succession of steps:
   a) depositing a first metal layer (12;25) over the entire surface of a chip;
   b) selectively etching the first metal layer (12;25) to form desired patterns of metal interconnection lines between components previously defined;
   c) depositing a layer (13) of passivating material over the entire surface of the chip;
   d) selectively etching the layer (13) of passivating material down to the first metal layer (12;25) to define bonding areas (14,15;27,28) represented by uncovered portions of the first metal layer (12;25);
   e) depositing a thick second metal layer (16;29) over the entire surface of the chip;
   f) selectively etching the second metal layer (16;29) down to the layer (13) of passivating material to remove the second metal layer (16;29) outside said bonding areas (14,15;27,28);
   g) connecting bonding wires (17,18;30,31) to the surface of the second metal layer (16;29) in correspondance of said bonding areas (14,15;27,28).

2. A process according to claim 1, characterized in that said power semiconductor device is a power MOSFET.

3. A process according to claim 1, characterized in that said power semiconductor device is a PIC.

4. A process according to claim 1, characterized in that said power semiconductor device is an IGBT.

5. A process according to claim 1, characterized in that during step d) there is also provided the formation of isles (32) of passivating material inside at least one of said bonding areas (15).

6. A process according to any of the preceding claim, characterized in that at least one of said first metal layer (12;25) and second metal layer (16;29) is composed by an alloy of aluminium and silicon.

7. A process according to anyone of claims 1 to 5, characterized in that at least one of said first metal layer (12;25) and said second metal layer (16;29) is composed by an alloy of aluminium, silicon and titanium.

8. A process according to anyone of claims 1 to 5, characterized in that at least one of said first metal layer (12;25) and said second metal layer (16;29) is composed by an alloy of aluminium, silicon and copper.

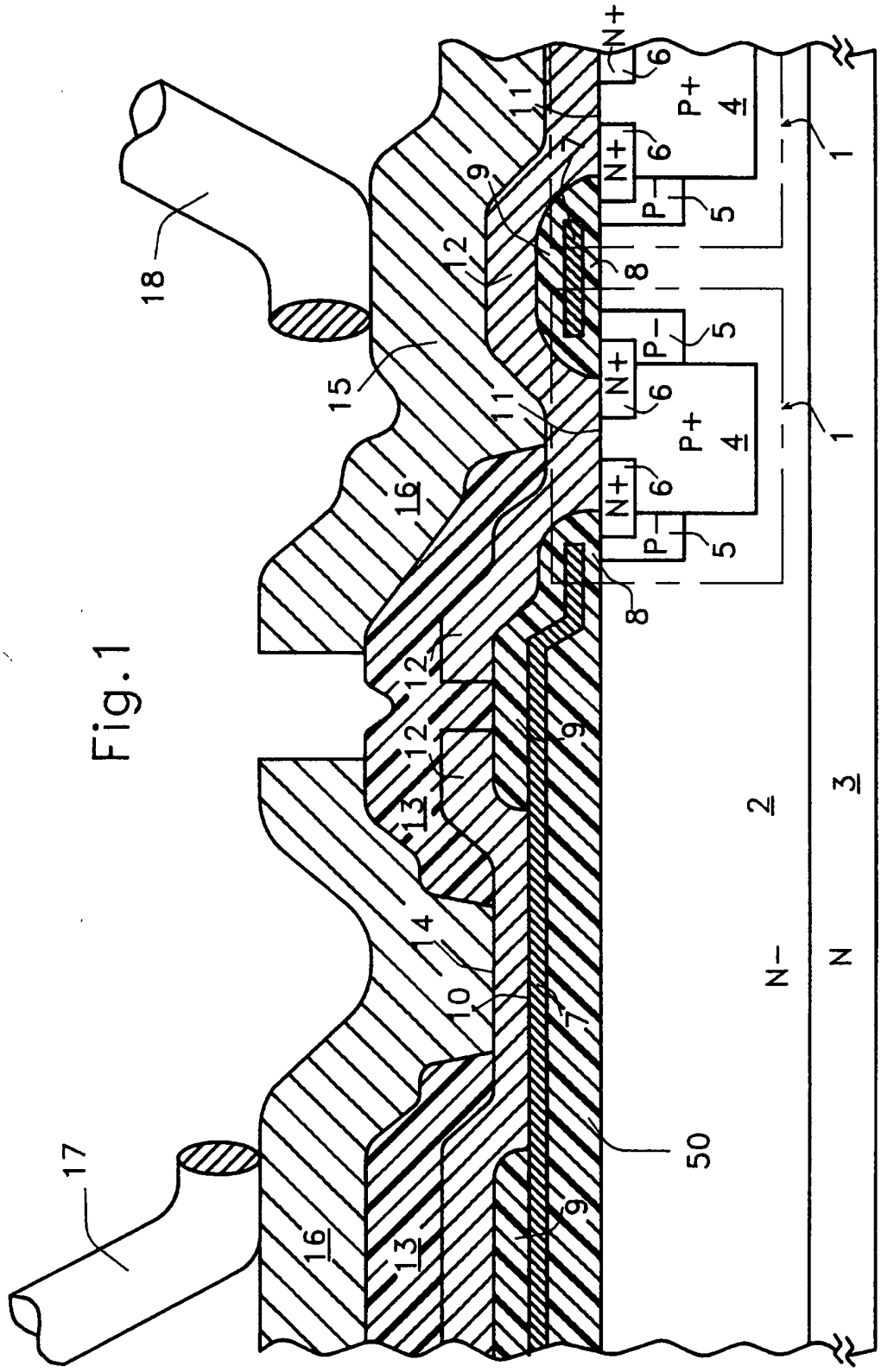
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Fig. 1

Fig.2

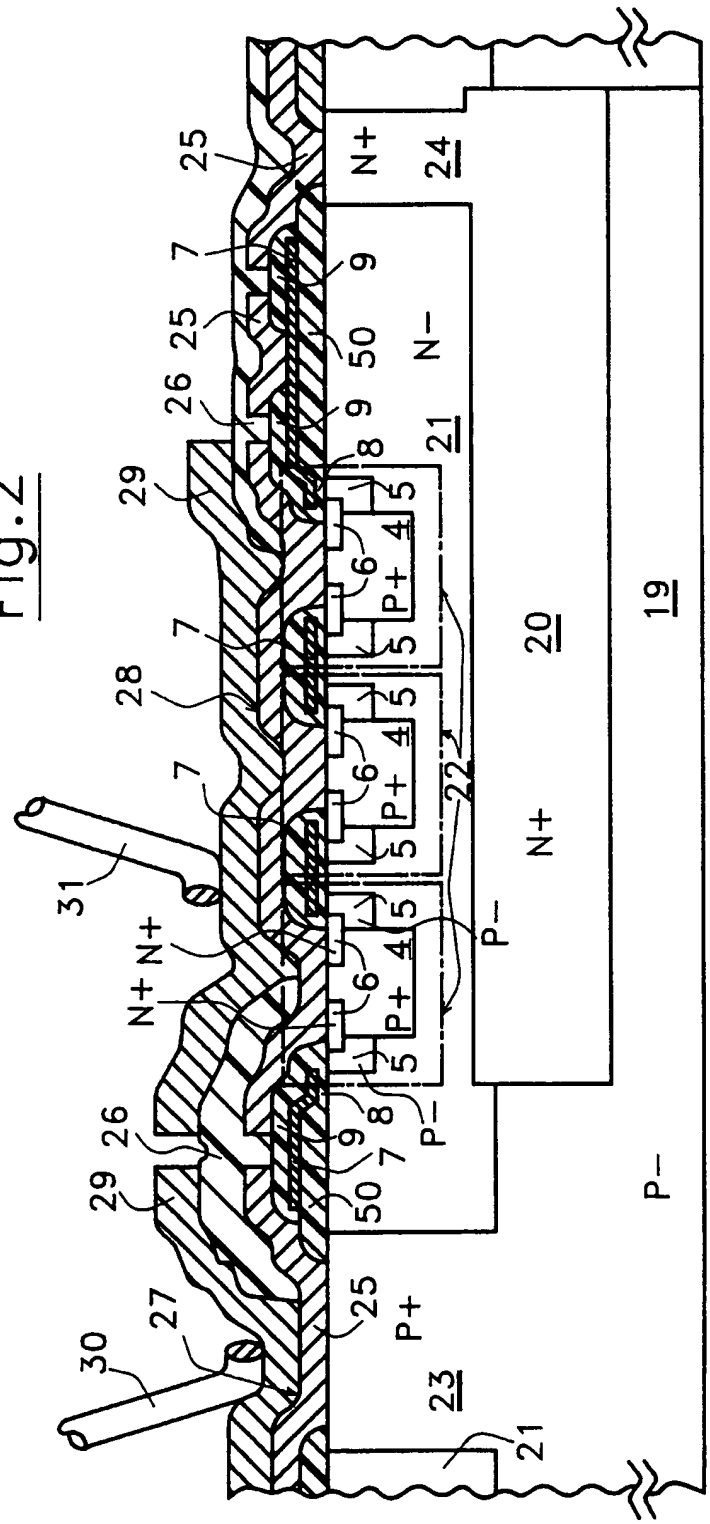
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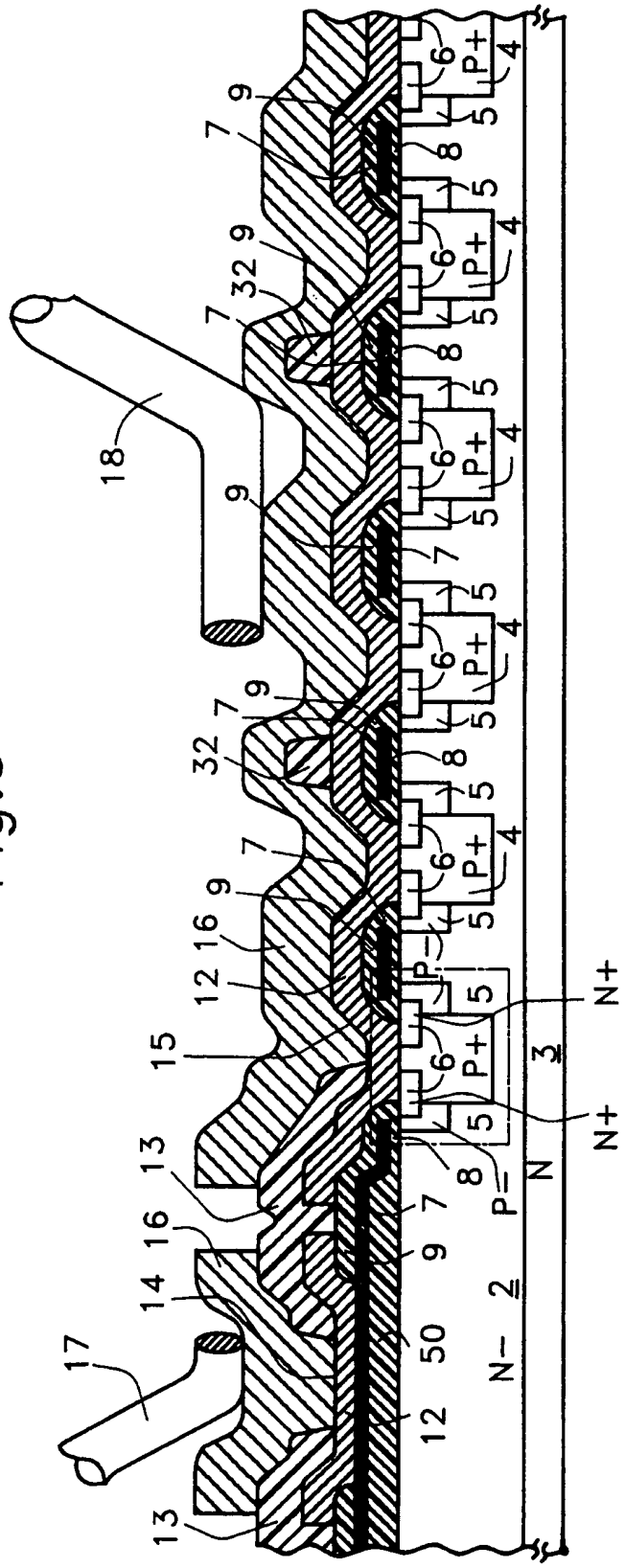
Fig.3



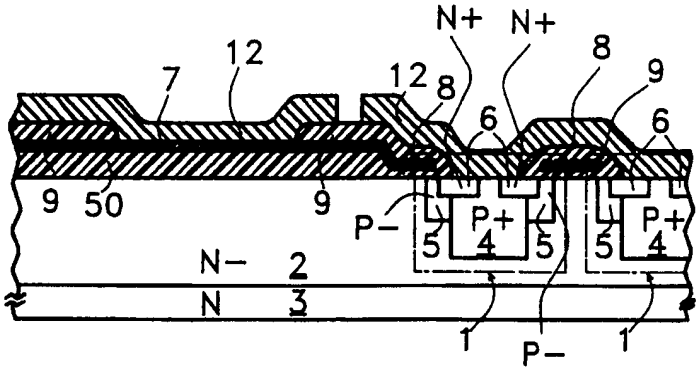


Fig.4

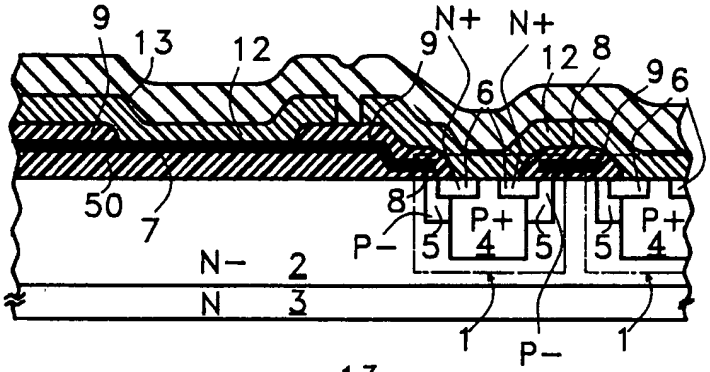


Fig.5

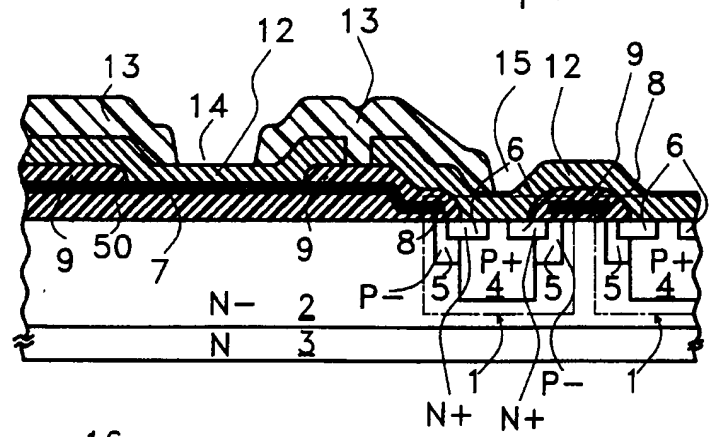


Fig.6

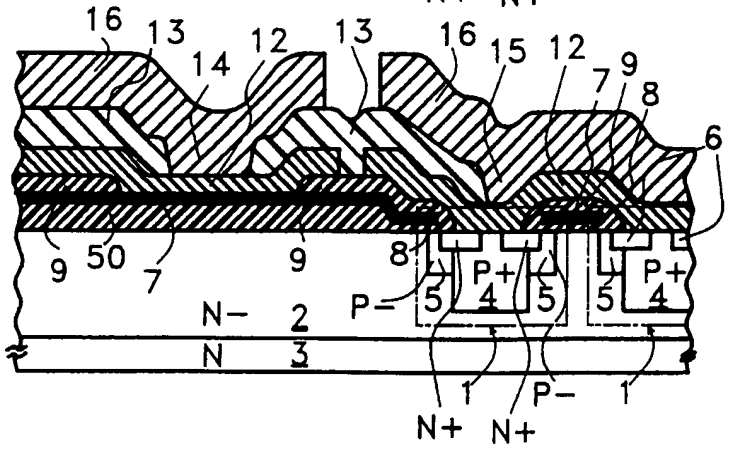


Fig.7

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EUROPEAN SEARCH REPORT

Application Number
EP 93 83 0396

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	WO-A-82 01102 (MOSTEK CORP) * page 6, line 1 - line 35 *	1	H01L23/482 H01L23/485 H01L21/768
A	EP-A-0 339 871 (ADVANCED MICRO DEVICES) * column 3, line 30 - column 4, line 36 *	1,6,8	
A	PATENT ABSTRACTS OF JAPAN vol. 13, no. 62 (E-715)13 February 1989 & JP-A-63 250 142 (NEC CORP)	1	
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 4 (E-229)25 February 1984 & JP-A-58 199 533 (HITACHI SEISAKUSHO KK) * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.6)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	28 February 1994	Greene, S

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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